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Efficient and Accurate Frequency Synthesizer Model for SoC Processors

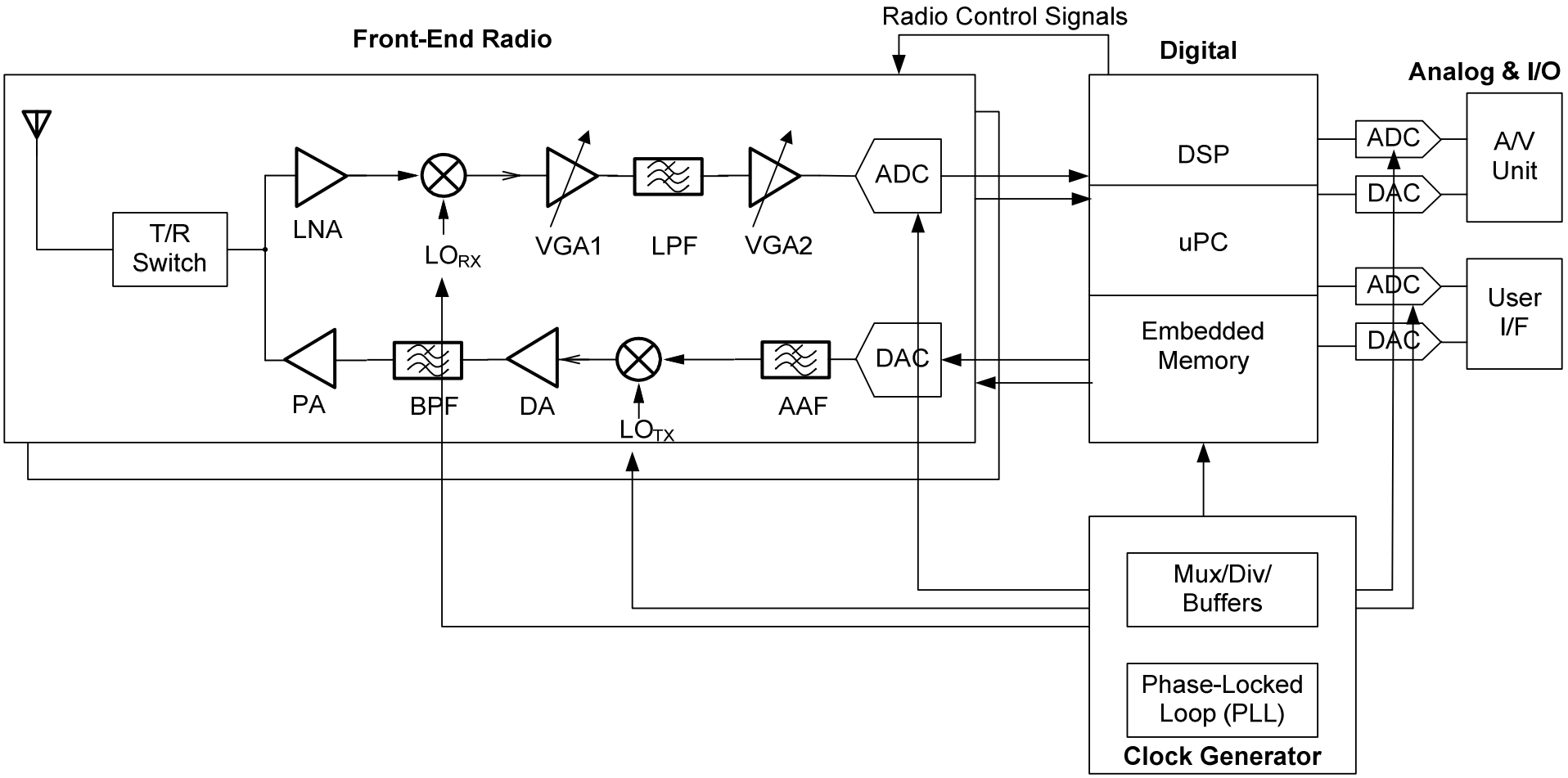
Dr. Amr Fahim
Semtech Corporation

Outline

- Target SoC Processors
- Frequency Synthesizers in SoC Processors
- Conventional Modeling Approaches
- Proposed Modeling Approach
- Simulation and Experimental Results

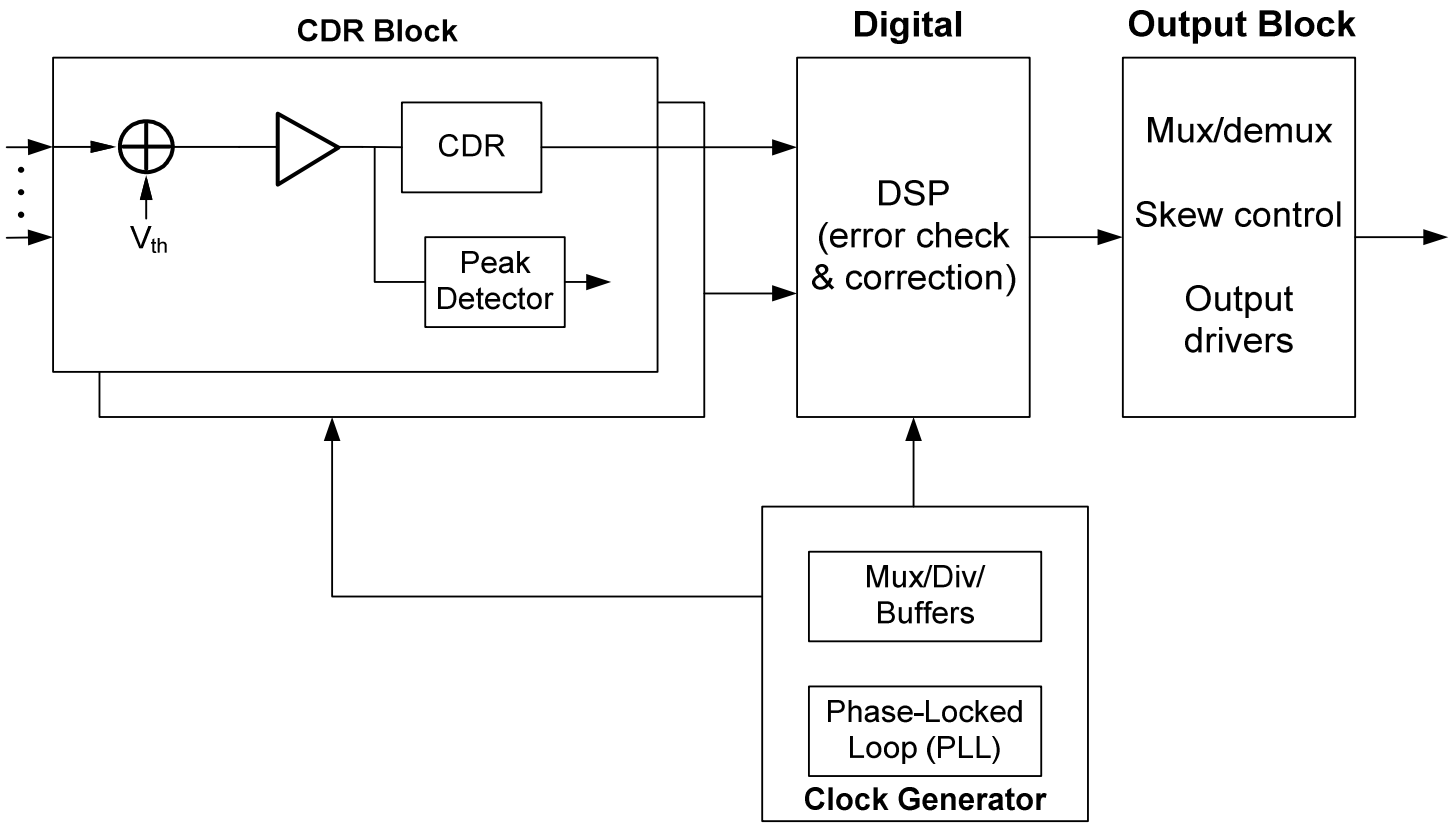
Target SoC Processors

- Typical RF SoC Processor:



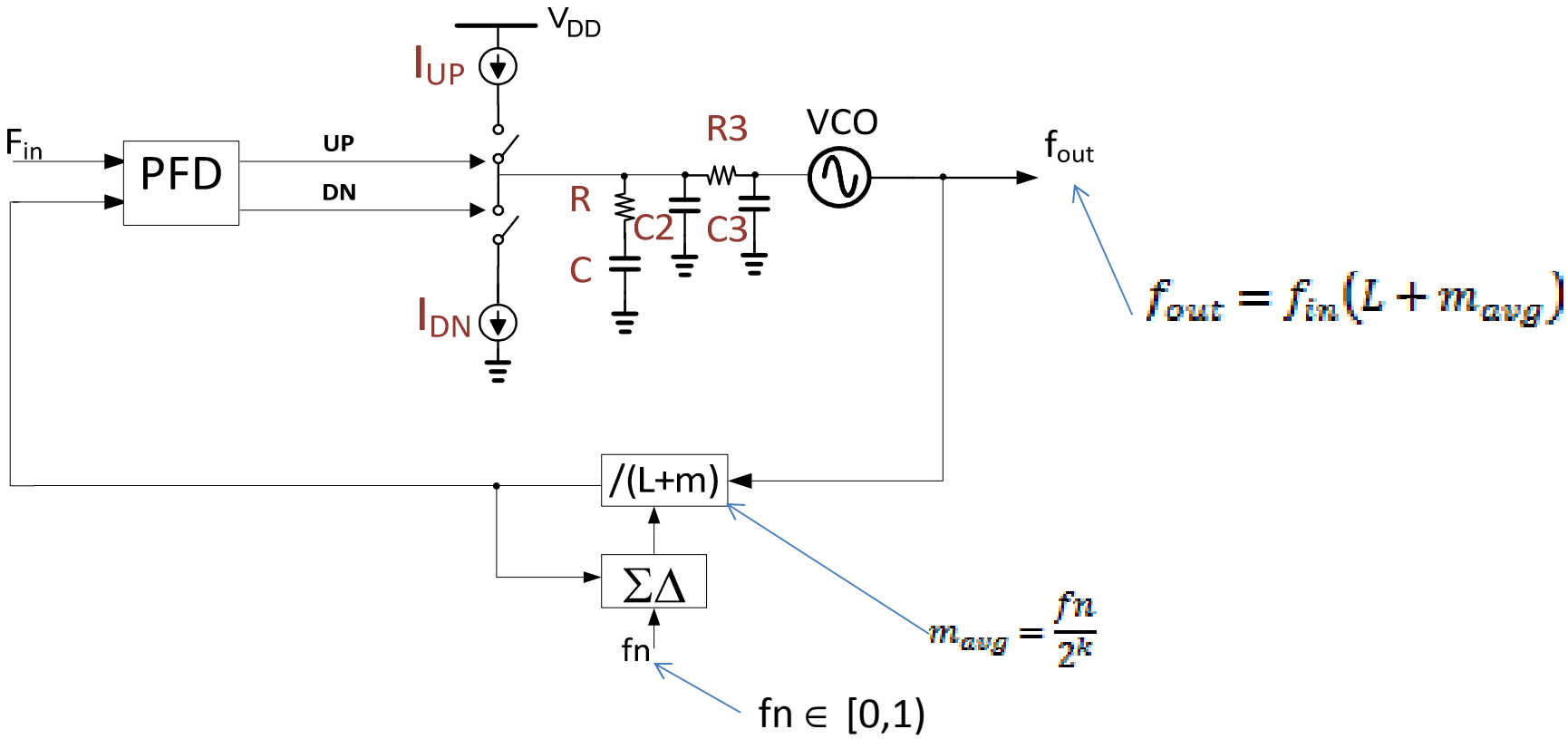
Target SoC Processors

- Typical Serdes SoC Processor:
  - Based on: SMI10031 (4:10 CDR Demux)



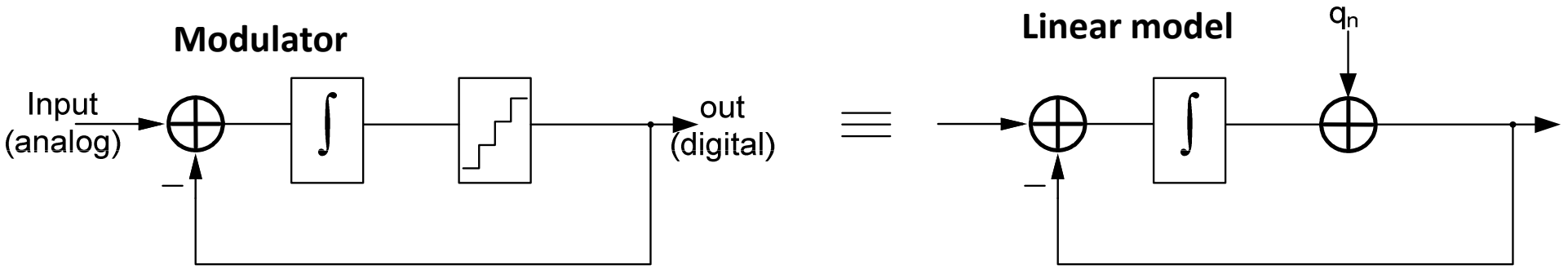
Frequency Synthesizers in SoC Processors

- ΣΔ Fractional-N Phase-Locked Loop (PLL)



Frequency Synthesizers in SoC Processors

- SD modulation basics:



STF → Low-pass filter
NTF → High pass filter

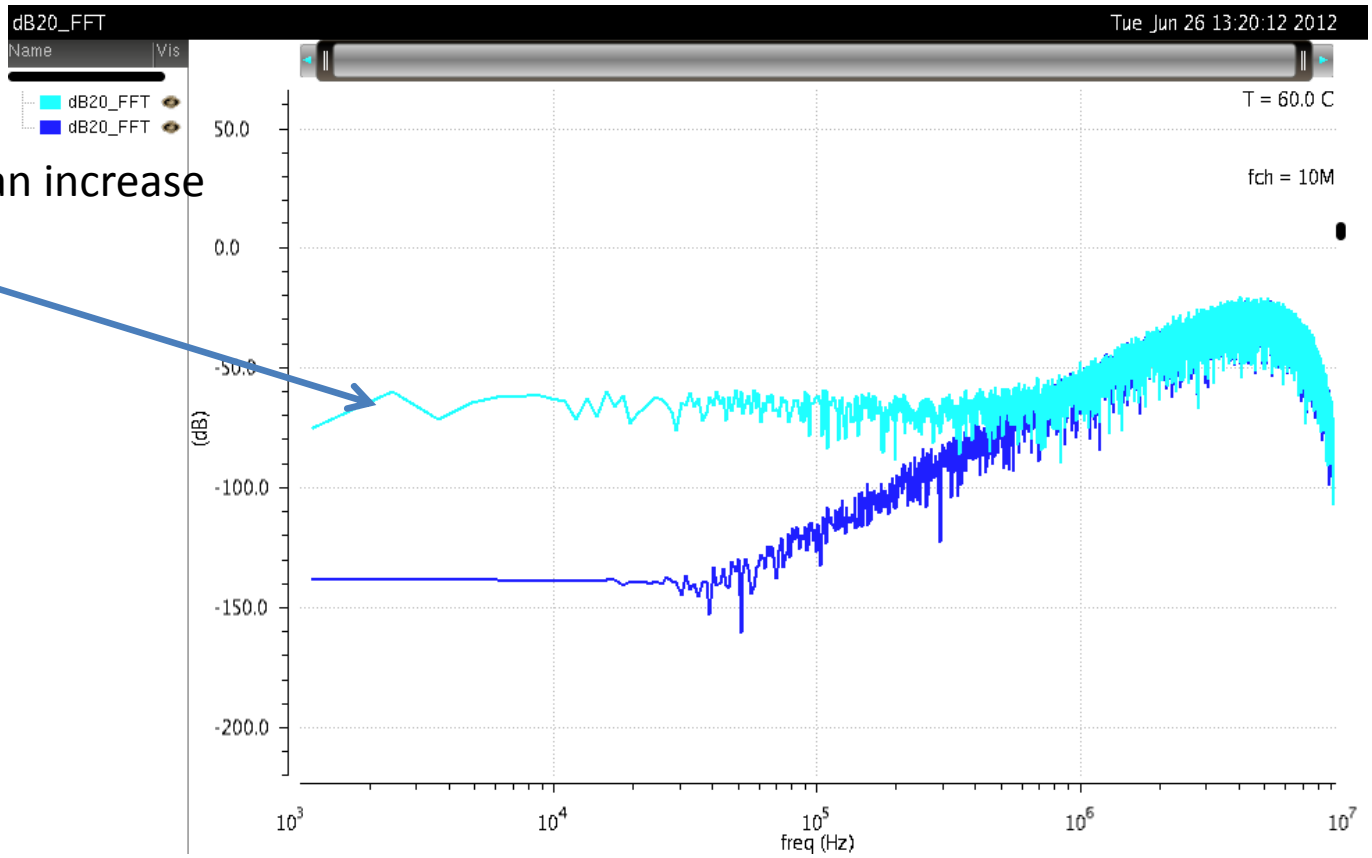
Quantization noise → additive white Gaussian noise only if step size is uniform

If step size is non-uniform, NTF shape breaks down.

Frequency Synthesizers in SoC Processors

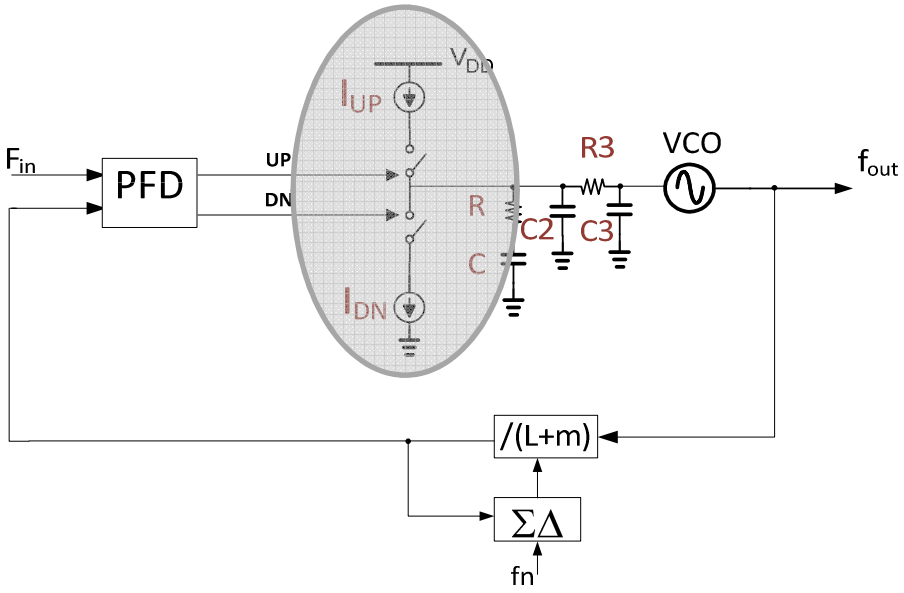
- Sigma-Delta Noise Folding:
  - Plot shows ideal (0%) and 2% mismatch
  - Nonlinearity causes high frequency quantization noise to fold back in-band

Noise folding causes an increase in in-band noise level

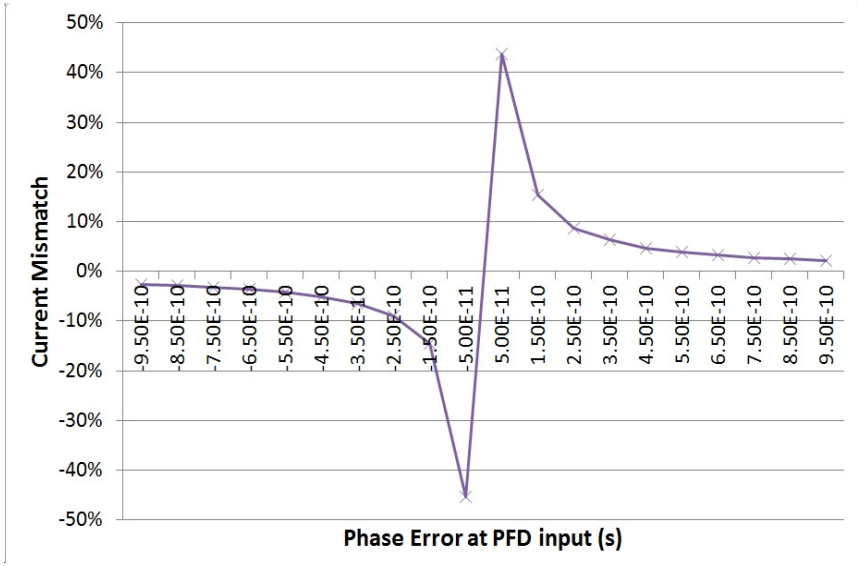


Frequency Synthesizers in SoC Processors

- Where does non-linear quantization noise steps arise in ΣΔ PLLs?
  - Charge pump current mismatch

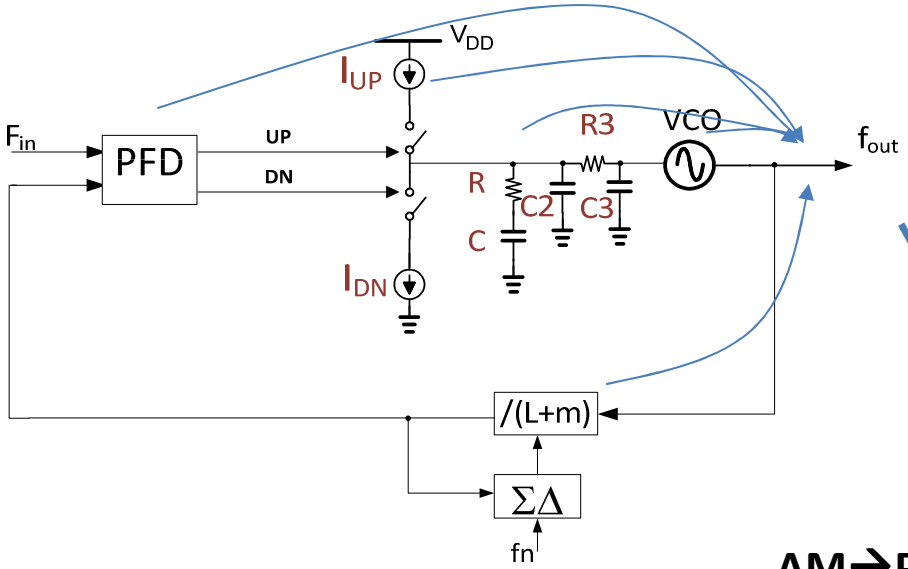


Charge pump dynamic current mismatch

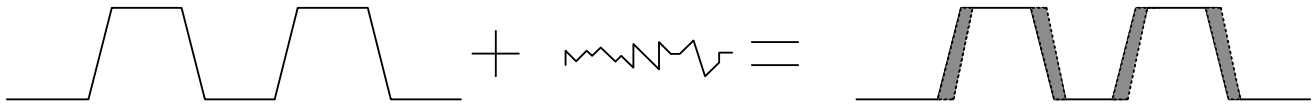


Frequency Synthesizers in SoC Processors

- PLL intrinsic noise is sum of noise sources of its components
- Jitter is the phase variation resulting from amplitude noise (AM→PM conversion of noise).

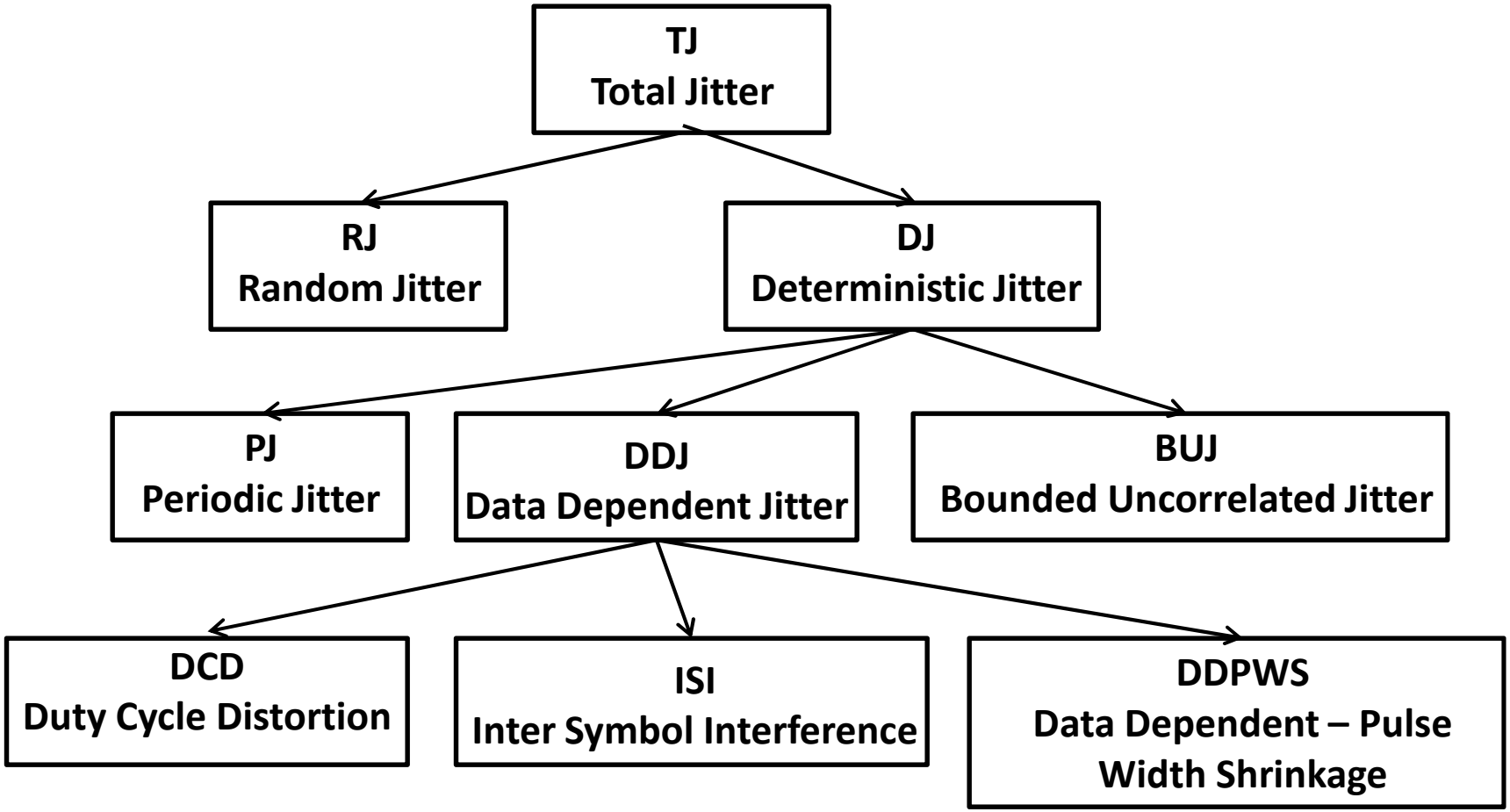


AM→PM conversion of noise



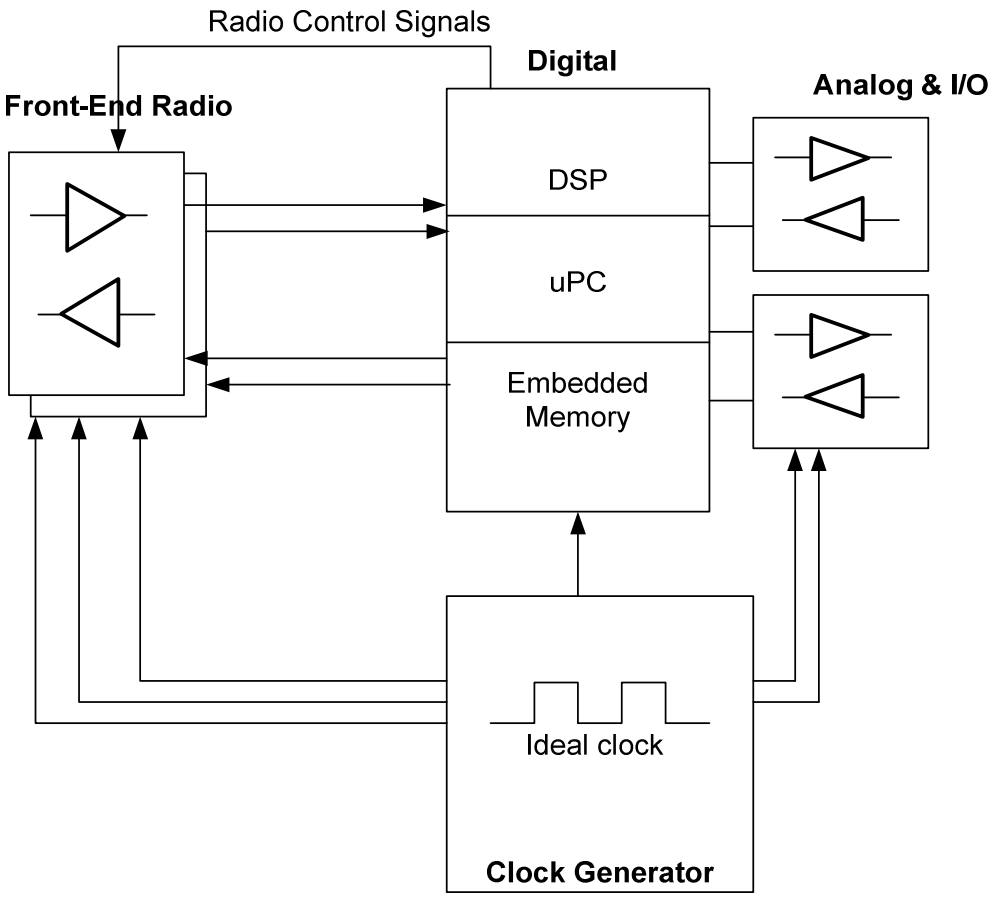
Frequency Synthesizers in SoC Processors

- Not all jitter created equal !



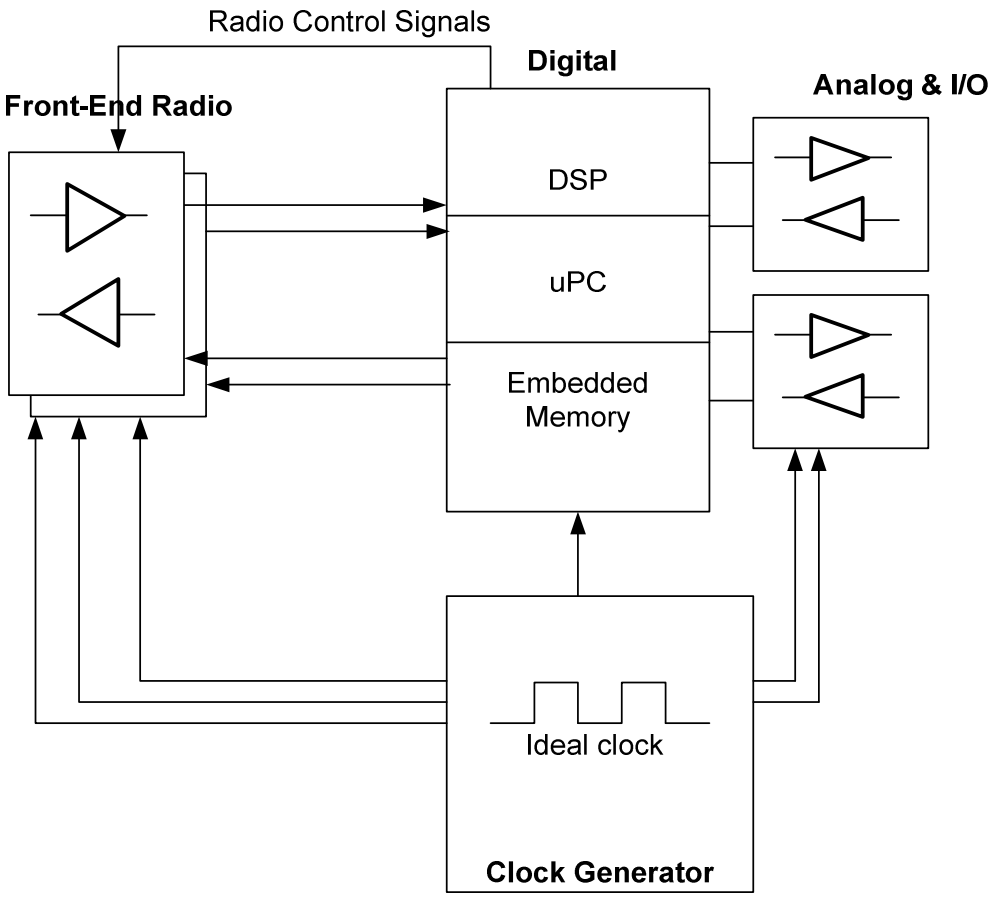
Conventional Modeling Approaches

- Level 0: Classical SoC Verification flow
  - Limited functional modeling of analog blocks
  - Ideal clock for frequency synthesizer
- Issues:
  - Maintenance and verification of analog models
  - Non-ideal analog effects ignored



Conventional Modeling Approaches

- Level 1: Analog Functional Verification Flow
  - Model analog blocks using Verilog-AMS
  - Frequency synthesizer ideal
- Issues:
  - Analog-centric flow – limited digital verification
  - How to simulate end-to-end verification in reasonable time?
  - Maintenance and verification of analog models

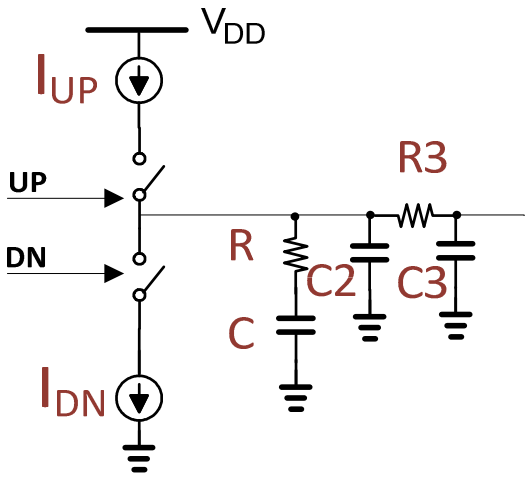


Proposed Modeling Approach

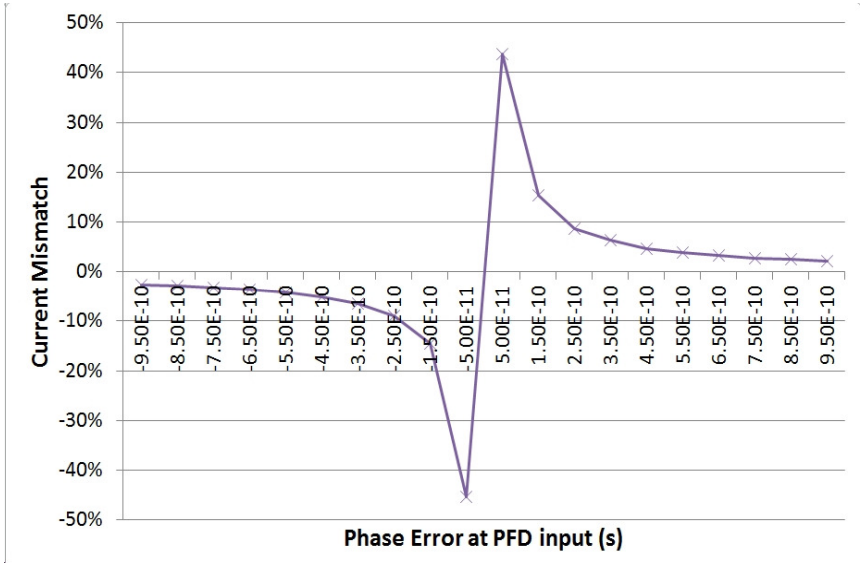
- Include analog effects in a Verilog-D model
  - This would include device noise
  - This would include analog non-linearities and non-idealities
  - Verilog is an event driven simulator → large speedups are now possible
- A phase-locked loop (PLL) is used to illustrate the modeling methodology
  - A parameterizable PLL model is implemented that would make maintenance straightforward
  - Main nonlinearity concern is the charge pump
  - Other non-idealities arising from the Verilog-D simulator are also addressed

Proposed Modeling Approach

- PLL Loop Filter and charge pump nonlinearity combined



Charge pump dynamic current mismatch



Steps:

1. **Curve fit charge pump nonlinearity**
2. **Compute the composite Laplace transform of charge pump + loop filter**
3. **Use Partial Fraction expansion to break into single terms**
4. **Apply inverse Laplace transform to the resulting terms (exponential terms result)**
5. **Use Taylor Series expansion of each exponential term and limit number of terms fast simulation time).**

Proposed Modeling Approach

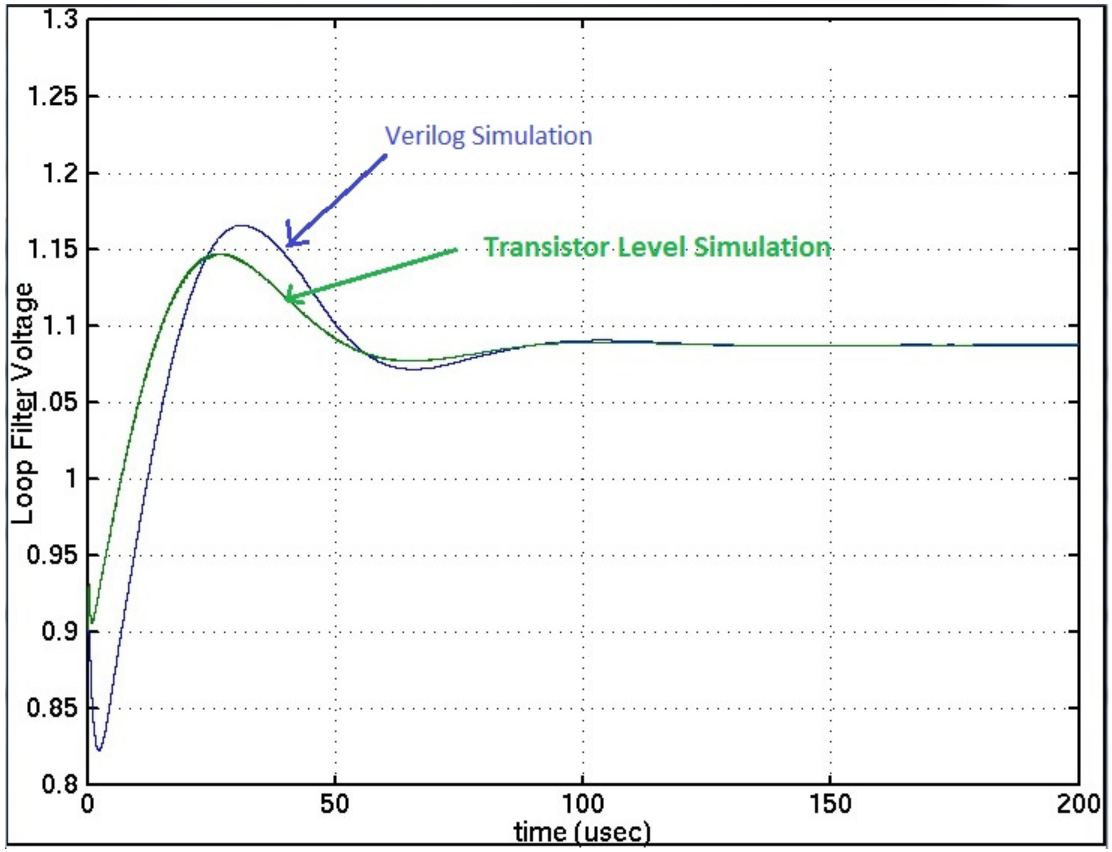
- Modified VCO model:
  - Verilog-D resolution is limited to 1fs
  - If VCO period is 250ps (4GHz frequency), the minimum increment in period is 250.001ps → minimum step size of 16kHz, too coarse for most applications (especially synchronous Gb Ethernet applications).
  - Proposed solution: dither periodically to obtain a fractional amount as required.
    - Measure the actual period and subtract from desired period
    - Accumulate this error, when it exceeds 1fs, subtract 1fs from this error and adjust the next VCO period to be larger by 1fs
  - The proposed solution introduces a spur in the output spectrum, but its magnitude is sufficiently low

Proposed Modeling Approach

- Noise modeling strategy:
  - Obtain noise numbers from transistor level periodic steady-state (pss) noise simulation of each PLL sub-block
  - Noise will be a composite of flicker and thermal noise
- Flicker noise:
  - Based on well-established and efficient Voss-McCartney algorithm to generate pink (1/f) noise densities (as well as $1/f^3$ for VCO up-converted flicker noise).
- Thermal Noise:
  - White noise, uniformly distributed
  - Verilog-D built-in function: $dist_normal()

Simulation Results

- Transient simulation validating Verilog-D model
  - Difference in behavior due to nonlinear varactor characteristic not being modeled in Verilog-D



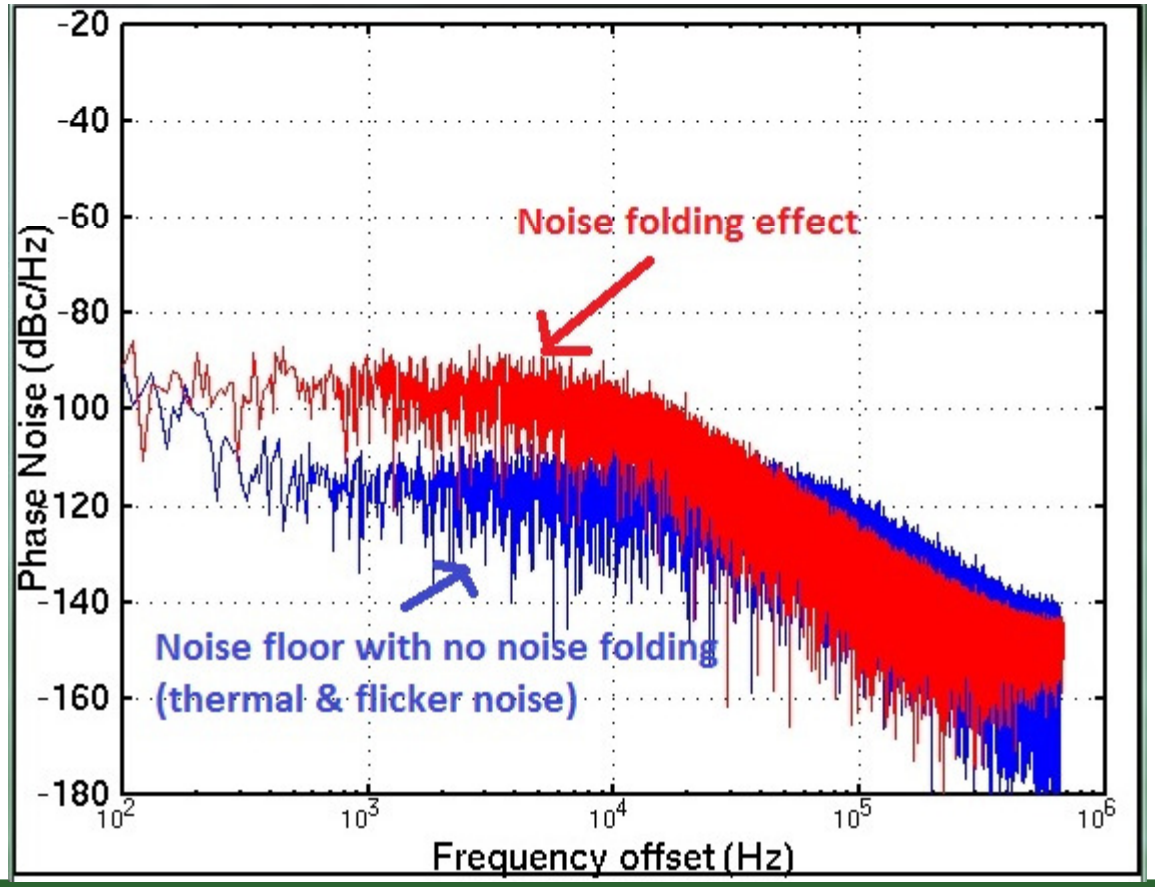
Simulation Results

- PLL Simulation Time:
  - 200usec transient simulation
  - Only Verilog-D model contains noise information
  - Using Icarus Verilog running on an Intel i7-2.4GHz machine

Model Type	Simulation Time
Transistor Level	1636 minutes
Verilog-A	36.3 minutes
Verilog-D	2.75 minutes

Simulation Results

- FFT of transient simulation with and without noise folding effect:
  - Linear & non-linear charge pump
  - 20ms transient simulation



Conclusions

- A novel modeling approach to frequency synthesizer modeling is demonstrated that is compatible with digital verification flows
- Non-linear noise folding effect in $\Sigma\Delta$ PLL frequency synthesizer is well predicted
- Noise models were also included to provide a full picture of total performance
- Modeling methodology can be extended to other analog/RF circuits

References

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